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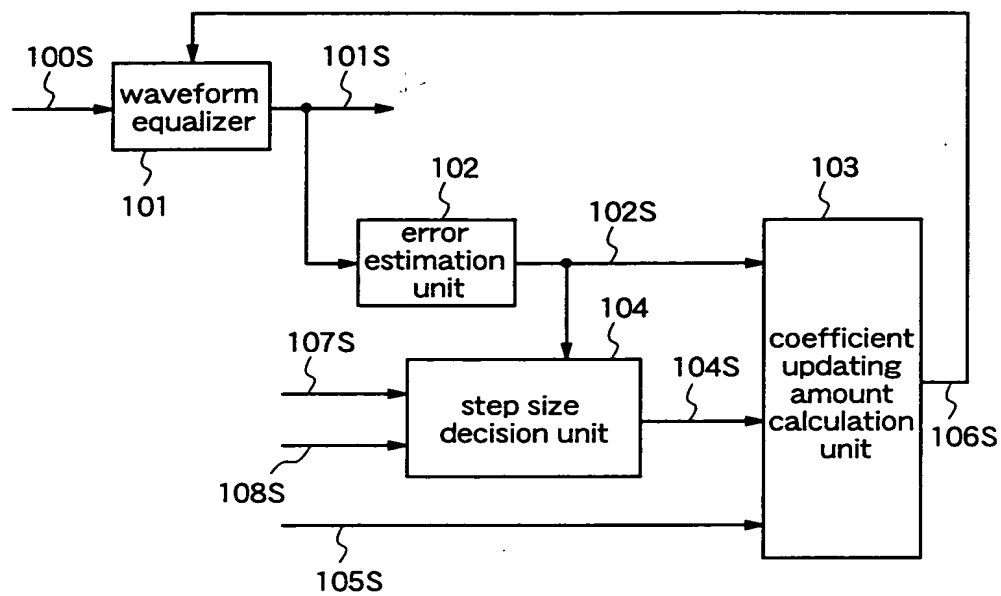


Fig.2

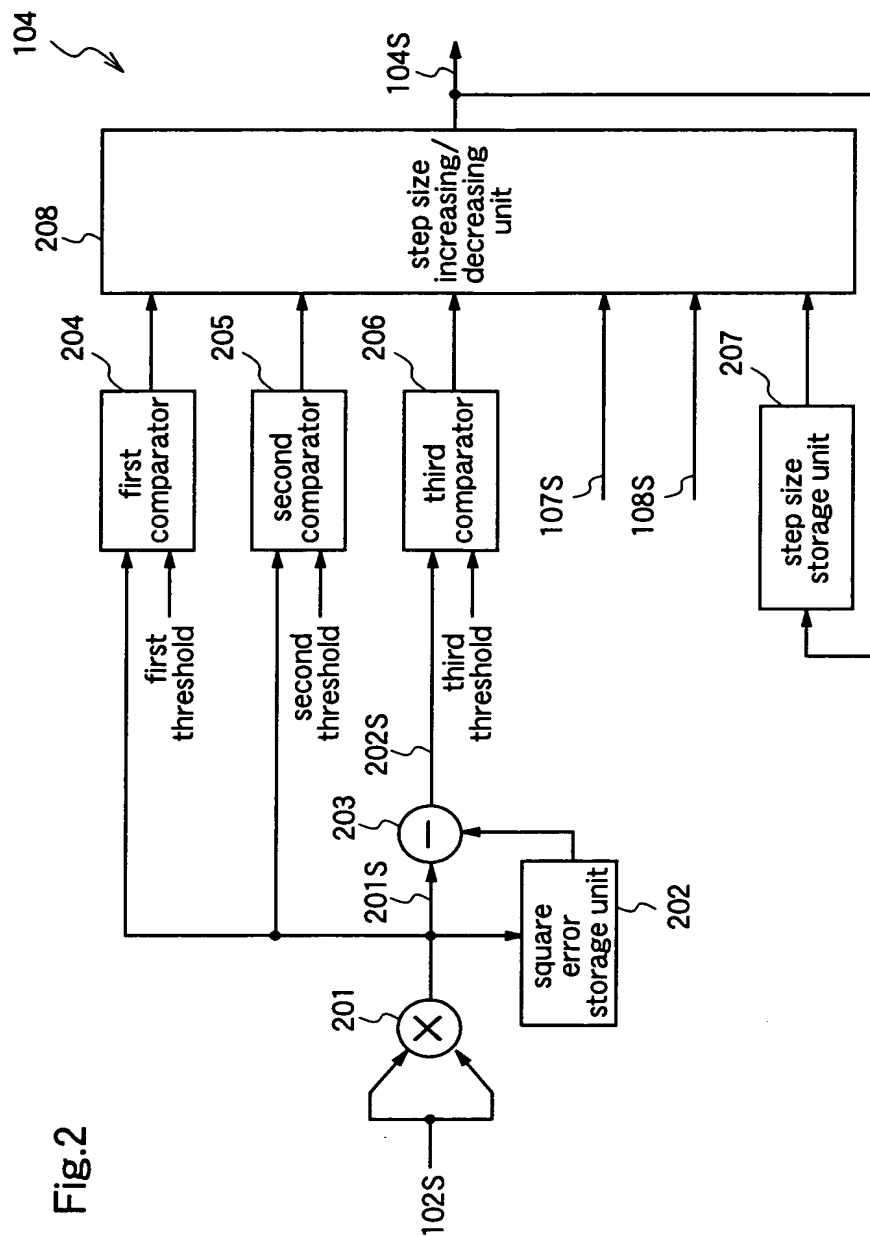


Fig.3

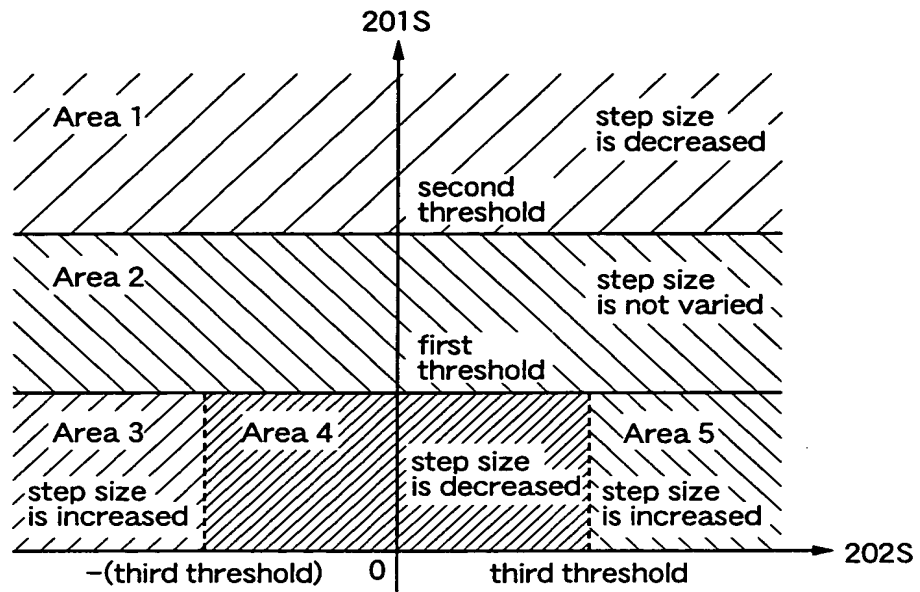
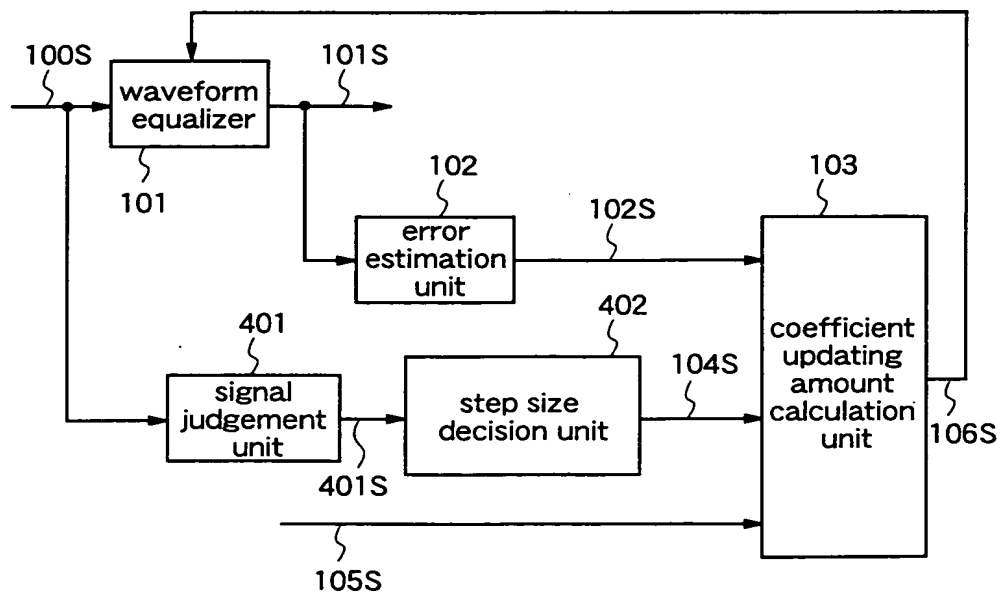


Fig.4



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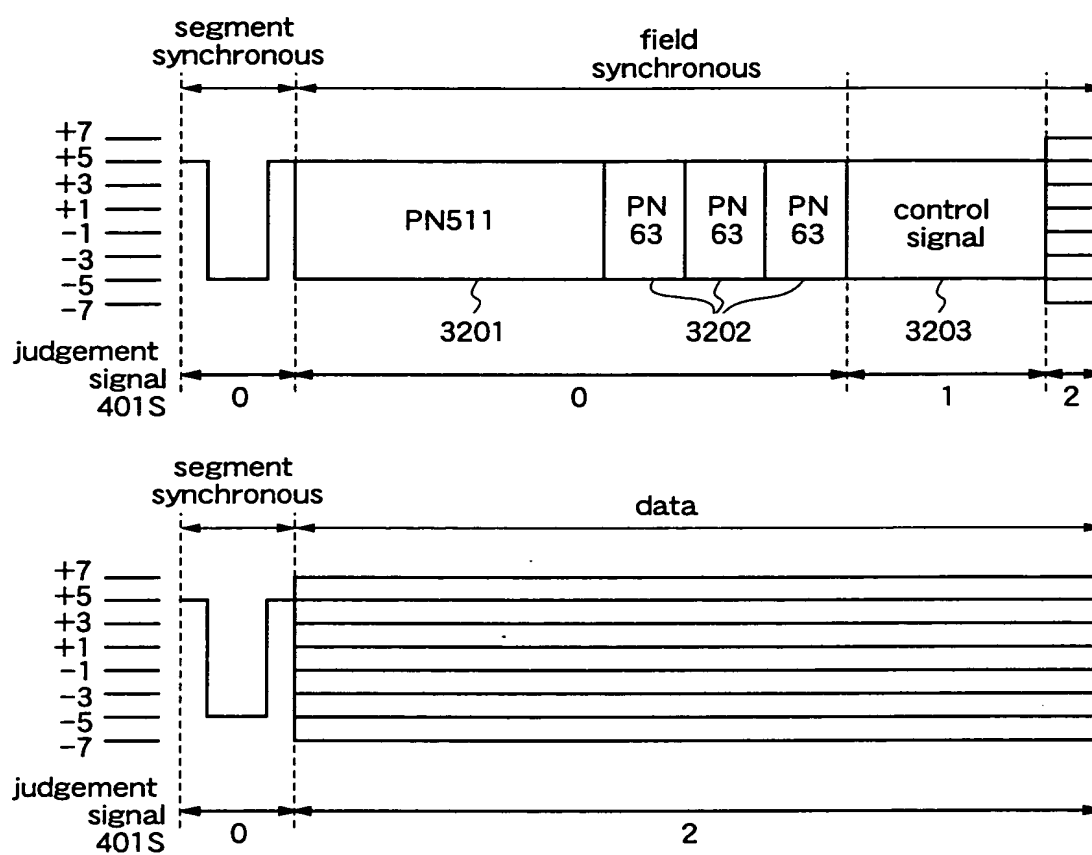


Fig.7

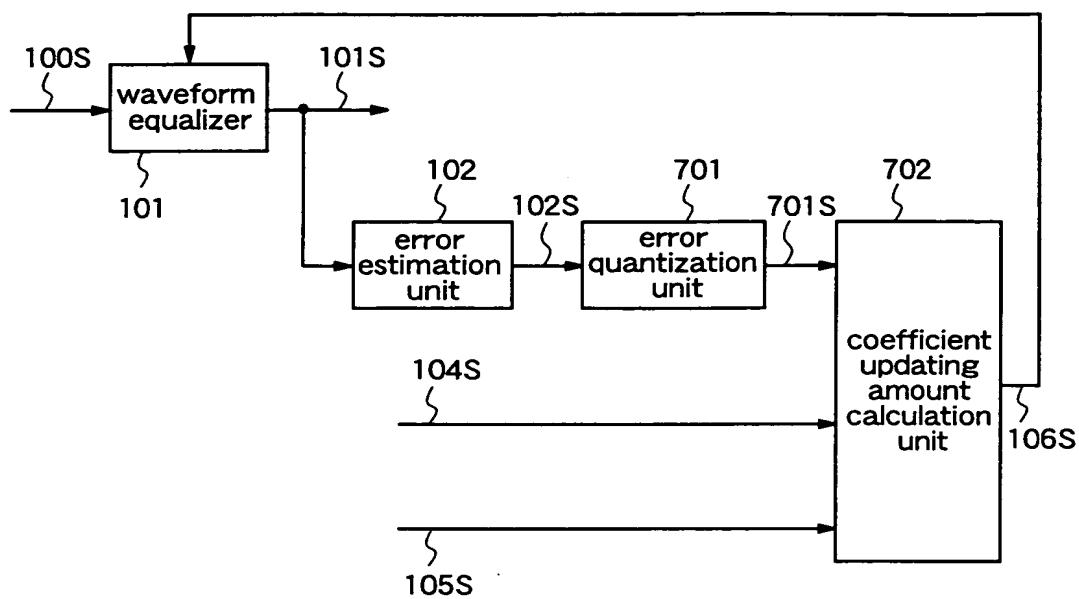


Fig.8

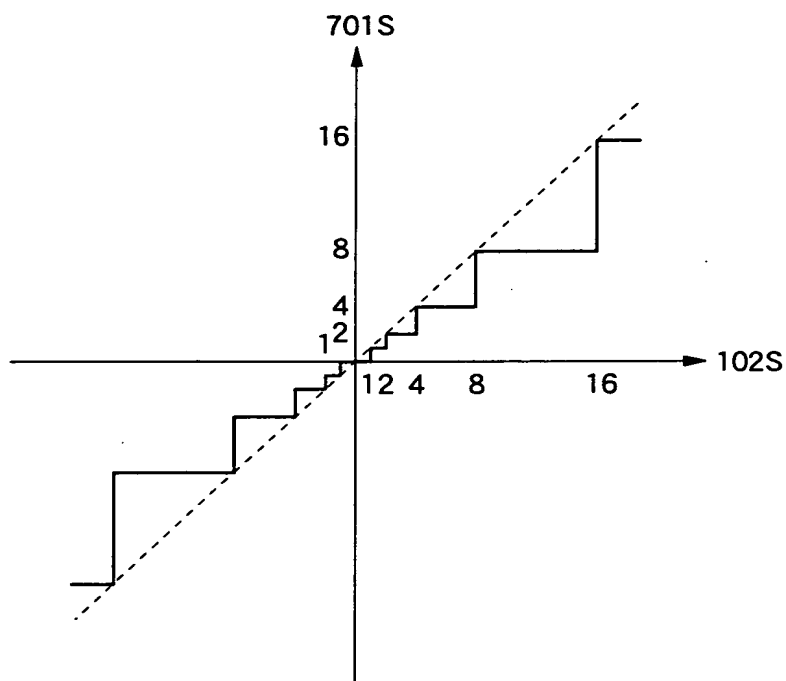


Fig.9

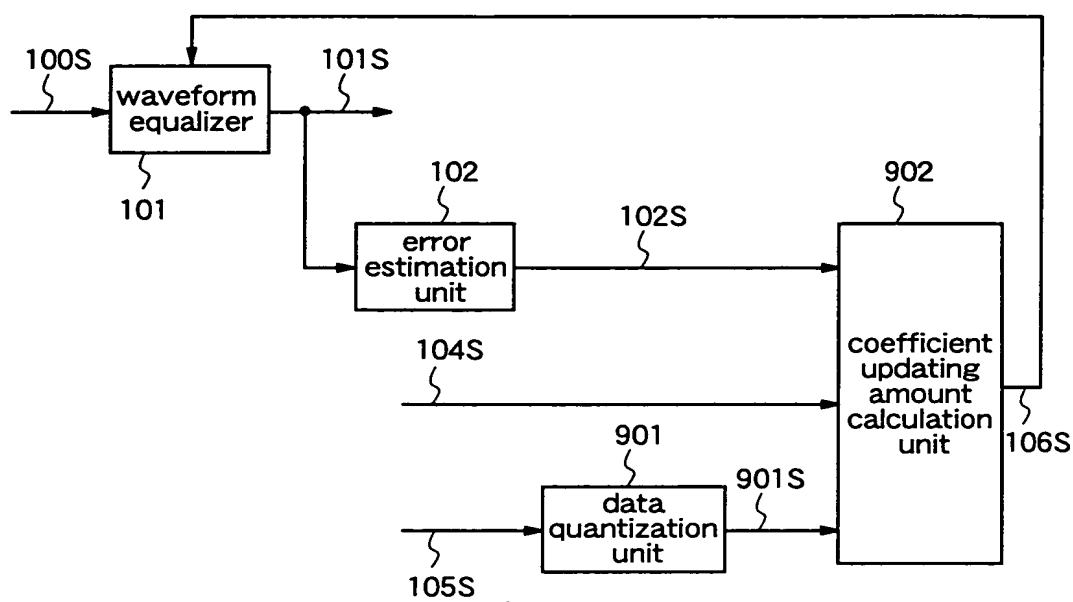


Fig.10

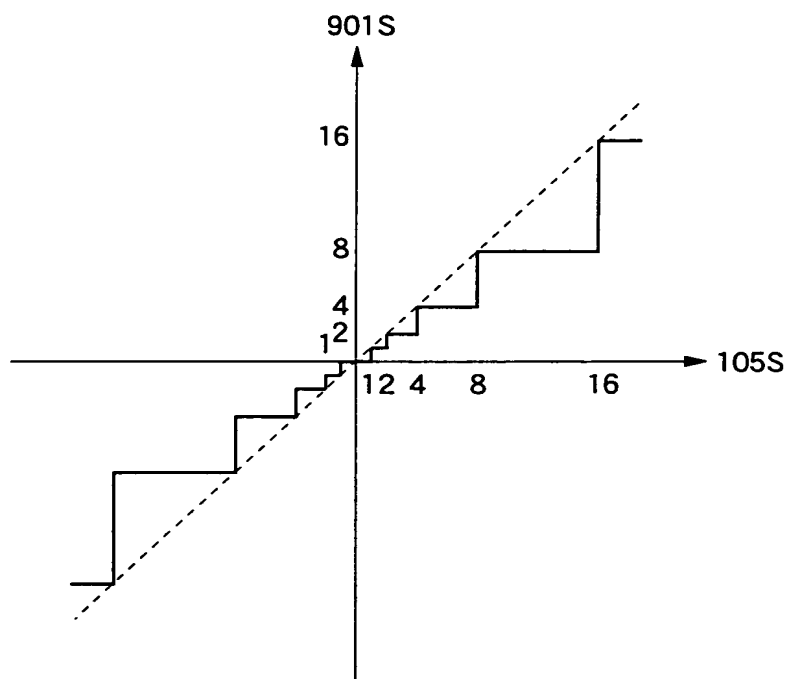


Fig.11

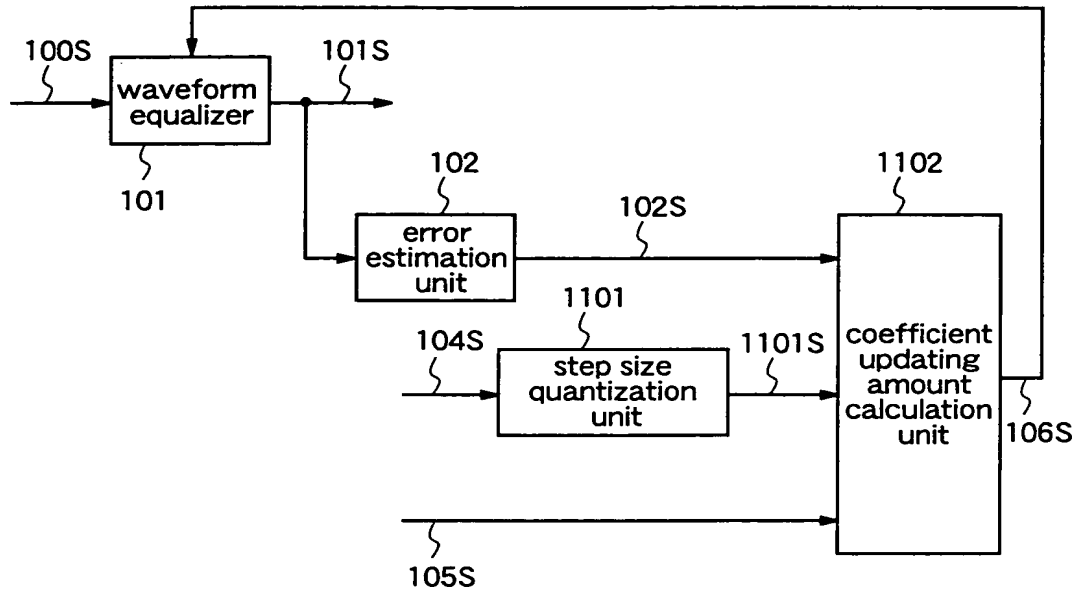


Fig.12

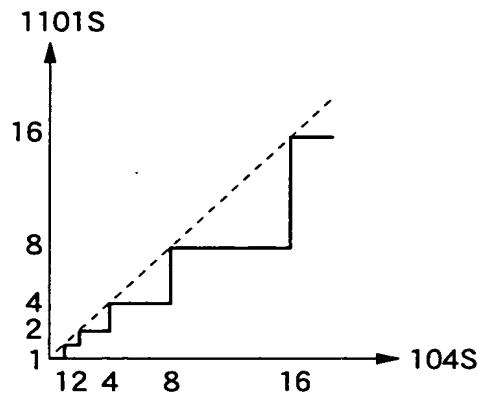
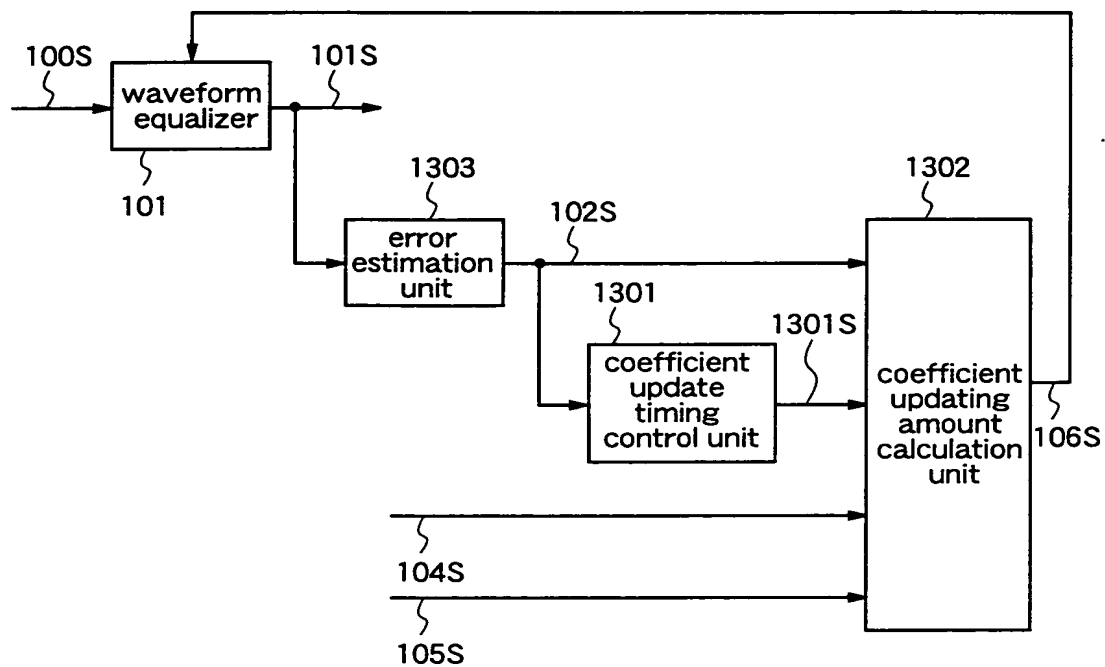


Fig.13



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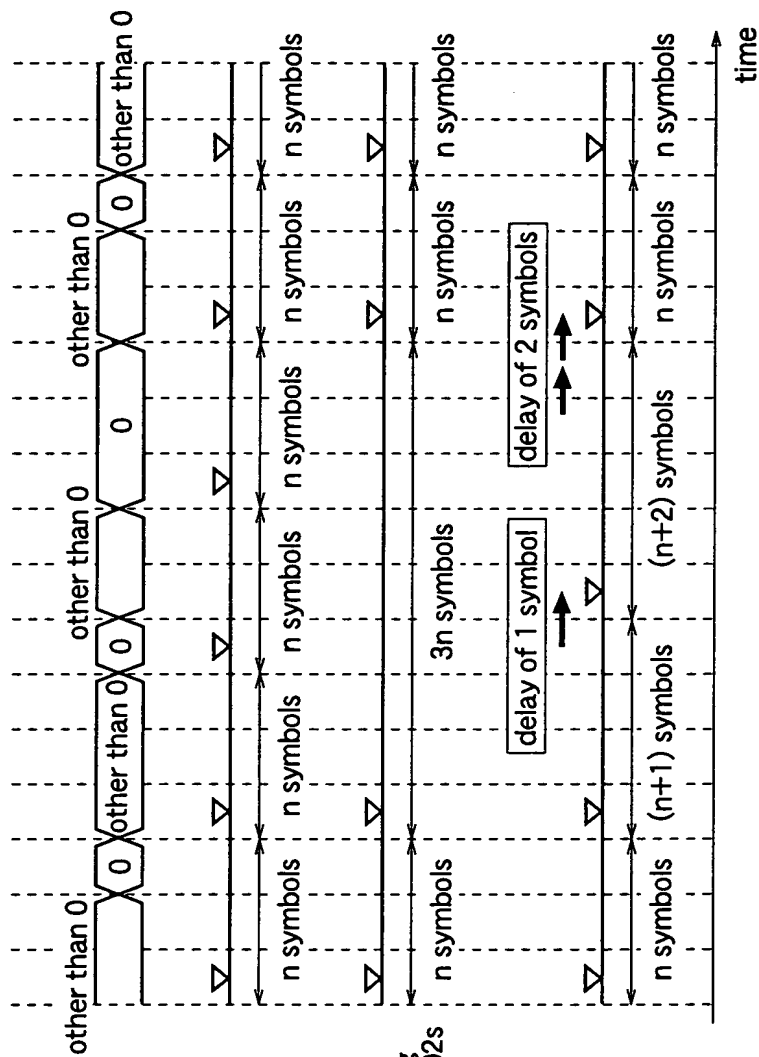


Fig.14 (a)
error signal 102s

Fig.14 (b)
prior art coefficient
update timing

Fig.14 (c)
prior art coefficient
update interval timing
for the error signal 102s
of other than 0

Fig.14 (d)
coefficient update
timing of the present
invention

Fig.15

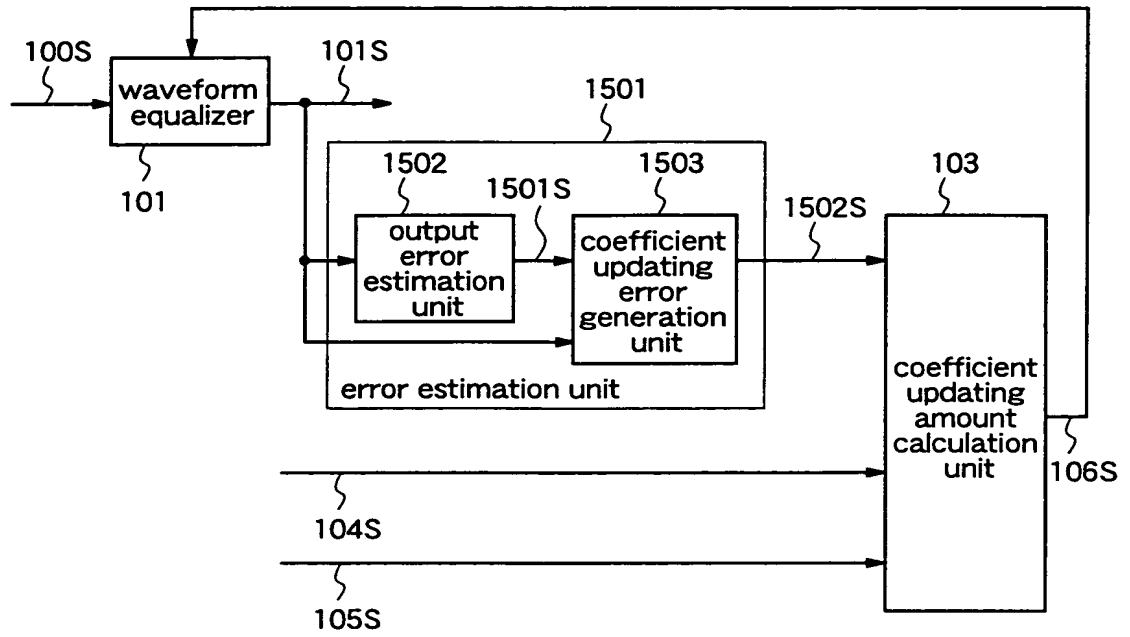


Fig.16 (a)

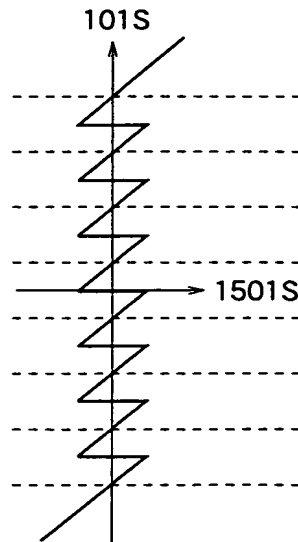


Fig.16 (b)

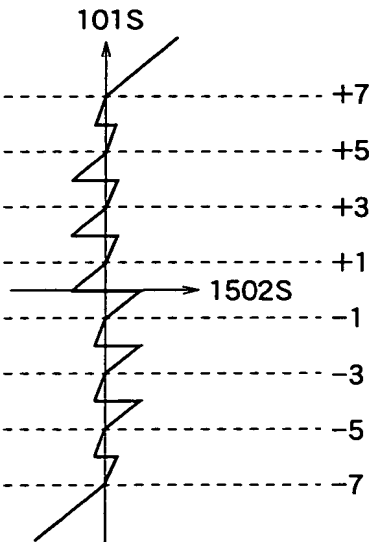


Fig.17

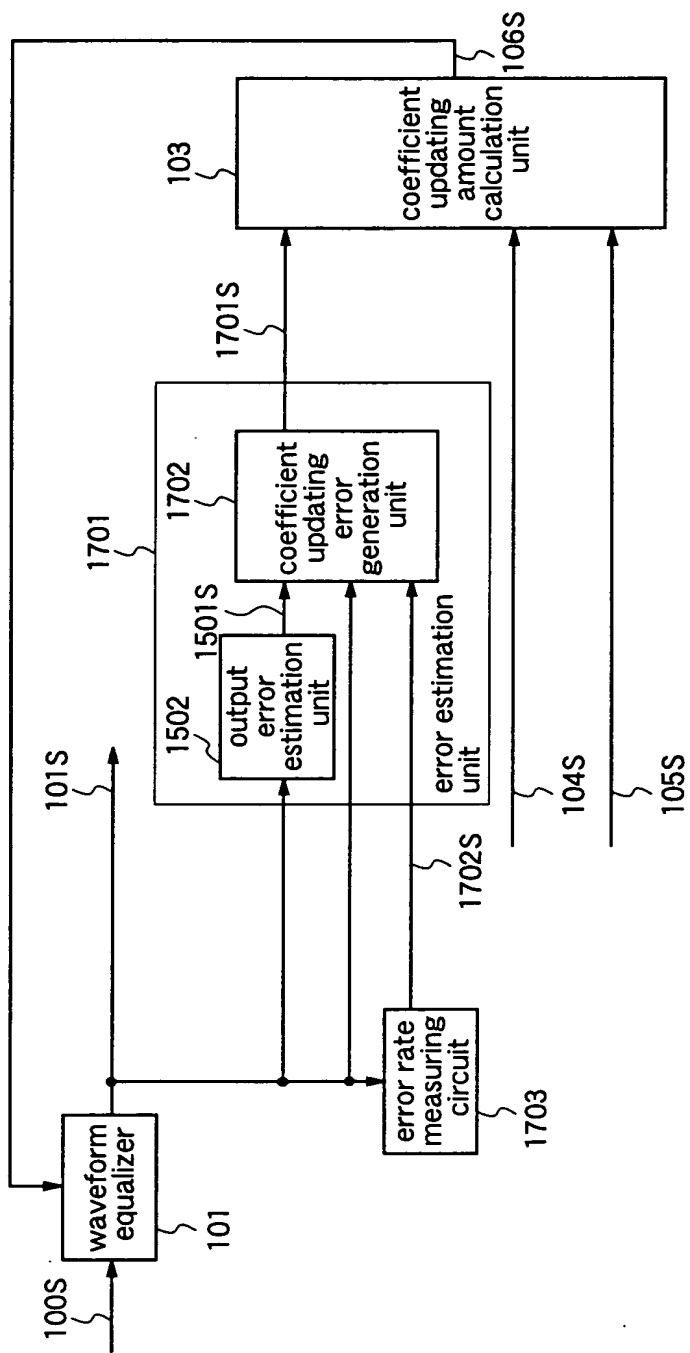


Fig.18 (a)

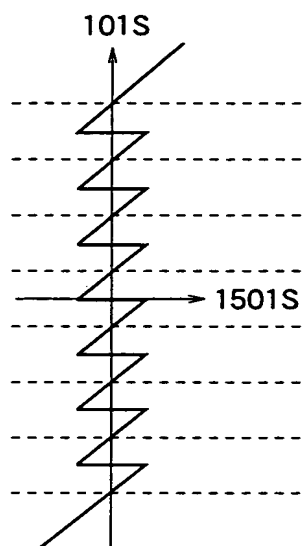


Fig.18 (b)

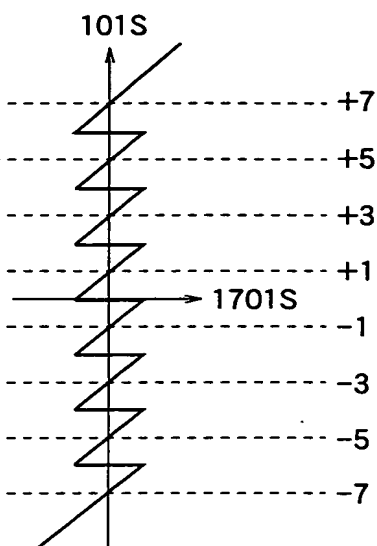


Fig.19 Prior Art

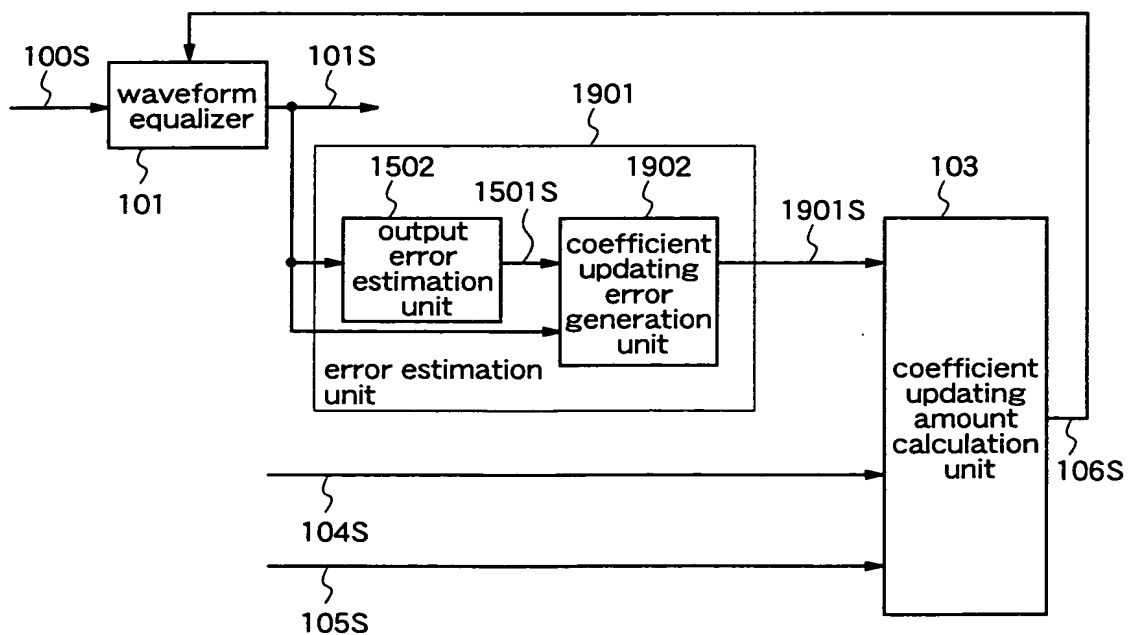
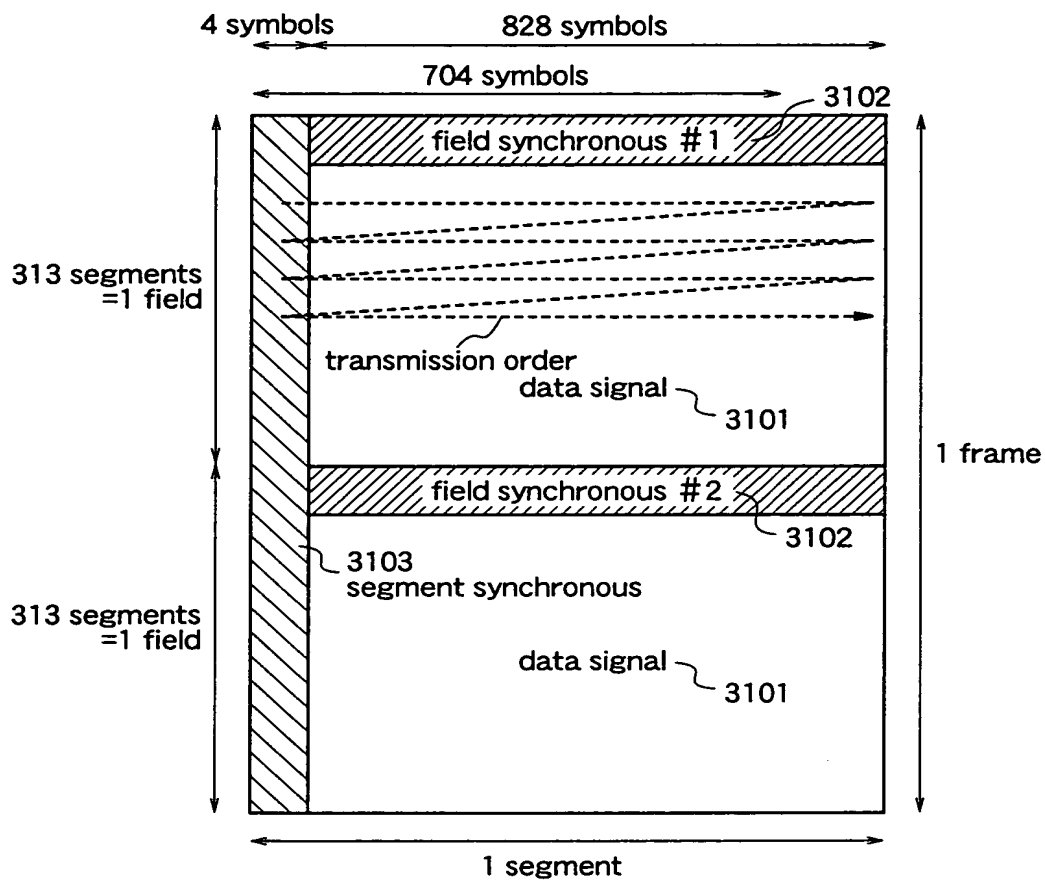


Fig.20



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Fig.21

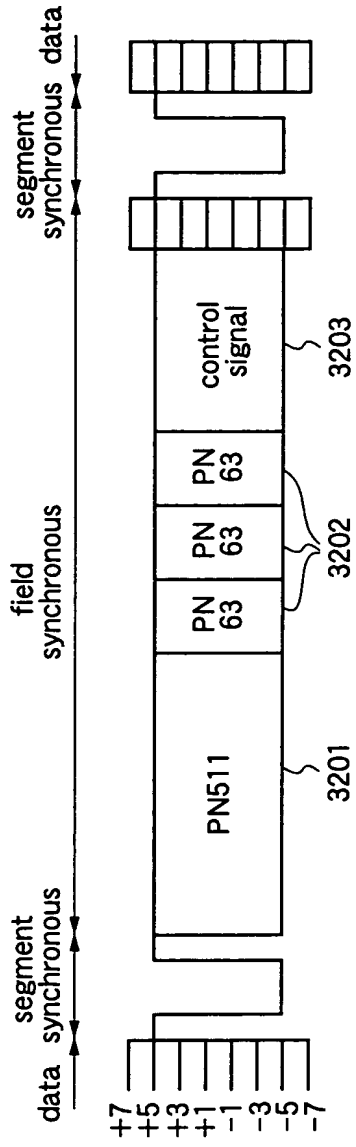


Fig.22 (b)



Fig.23

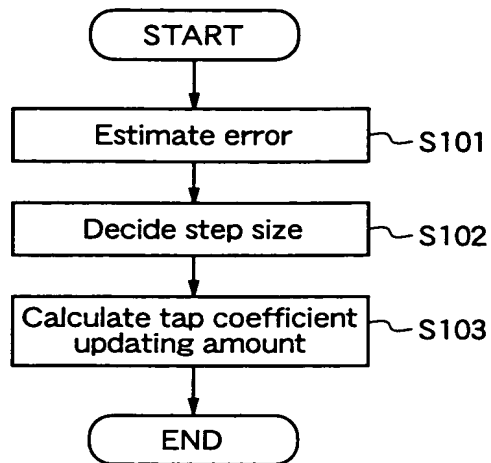


Fig.24

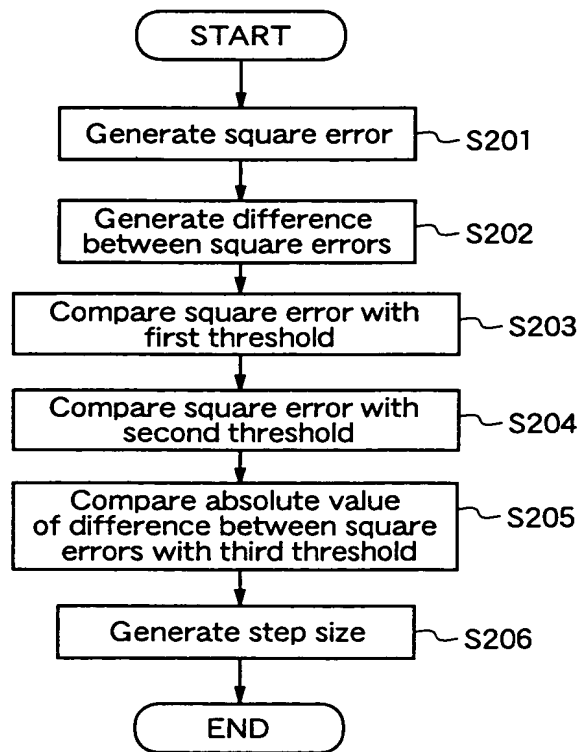


Fig.25

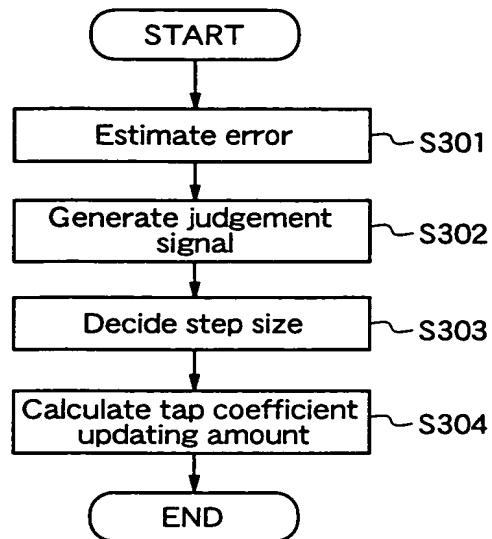


Fig.26

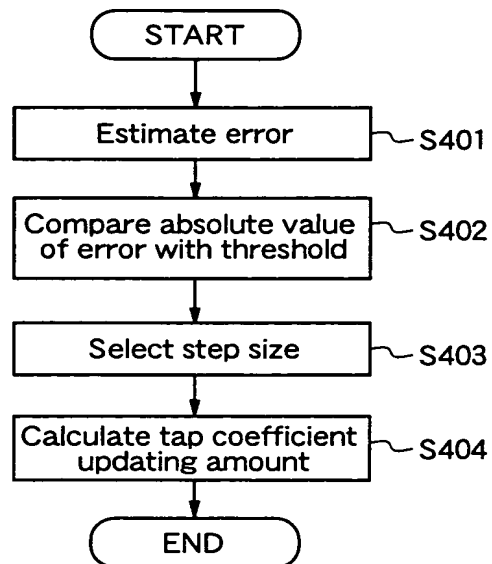


Fig.27

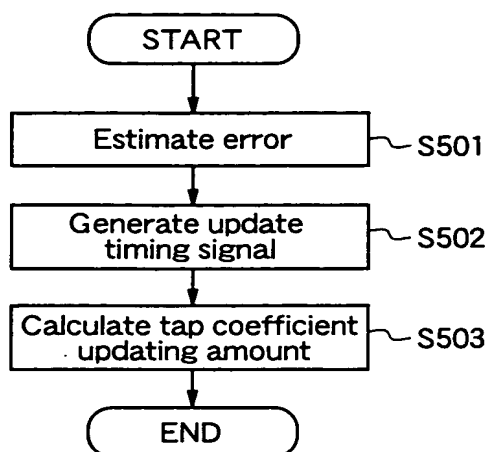
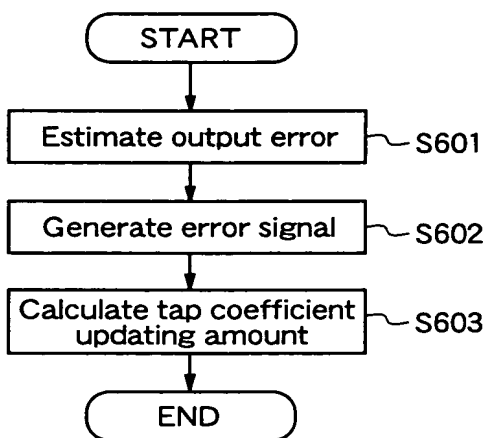


Fig.28





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